



AEROSPACE SYSTEMS DIVISION

DEFENSE ELECTRONIC PRODUCTS • RADIO CORPORATION OF AMERICA

April 26, 1967

Mr. Theodor H. Nelson
Harcourt, Brace & World, Inc.
757 Third Avenue
New York 17, New York

Reference: Your letter dated April 12, 1967

Dear Mr. Nelson:

Thank you for your interest in the Aerospace Systems Division of RCA with respect to airborne/spaceborne computers.

Per your request, I am enclosing a description of our Variable Instruction Computer (VIC), which has completed development. I hope this description will meet your present requirements.

If you have any further questions, please feel free to call me any time at (617) 272-4000, extension 2293.

Sincerely,

RADIO CORPORATION OF AMERICA
(Defense Electronic Products)

C. D. Beal
Data Processing, Marketing
Aerospace Systems Division

CDB/pmc
Enclosure

RELIABILITY ASPECTS OF THE
RCA/USAF VARIABLE INSTRUCTION COMPUTER

by

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This paper is intended to show how the unique features of the Variable Instruction Computer (VIC) make it valuable for applications requiring high reliability. By careful choice of components, use of error checking circuits, and selected application of redundant hardware, the basic unextended reliability of the VIC is comparable with the state-of-the-art. This is verified by a standard MIL-HDBK-217 type of analysis.

The variable instruction technique is briefly described by use of a block diagram. The method for extending reliability by use of variable instructions is explained and an example is given. The concept of algorithm change to achieve controlled graceful degradation is discussed. An analysis of a typical application of this technique is given and extensions of the variable instruction concept to more advanced reliability requirements are discussed.

Introduction

The Variable Instruction Computer (VIC) is a joint RCA and USAF development which provides the aerospace computer user with a high degree of flexibility, modularity, and reliability. Under an R&D program AF 33-(615)-2588 sponsored by the Avionics Laboratory, Wright-Patterson Air Force Base, RCA was funded to build a research model which would demonstrate some of RCA's VIC concepts. This paper describes that research model and discusses the reliability aspects of the VIC.

VIC Concept

First, what is the variable instruction concept? The key word is variable, which means within a single order class the variations may include:

1. the source of the information
2. the function performed on this information
3. the destination of the results.

The variable instruction tool provides the programmer with the hardware flexibility to combine, in many possible ways, the variations in

information sources, functions, and destinations. This flexibility is in contrast with the conventional computer which forces the programmer to use the instruction set wired into machine. The result is a compromise which is usually less than optimum for the application. Figure 1 compares the steps involved in a conventional computer with those used in the VIC. In the VIC, the macro order specified a micro order sequence and modifies the source and destination of the data. The micro order sequence is a series of discrete steps which sets up transfer paths, assigns registers, controls shifts, sets patterns of logical operations, controls arithmetic operations, sets counts and tests.

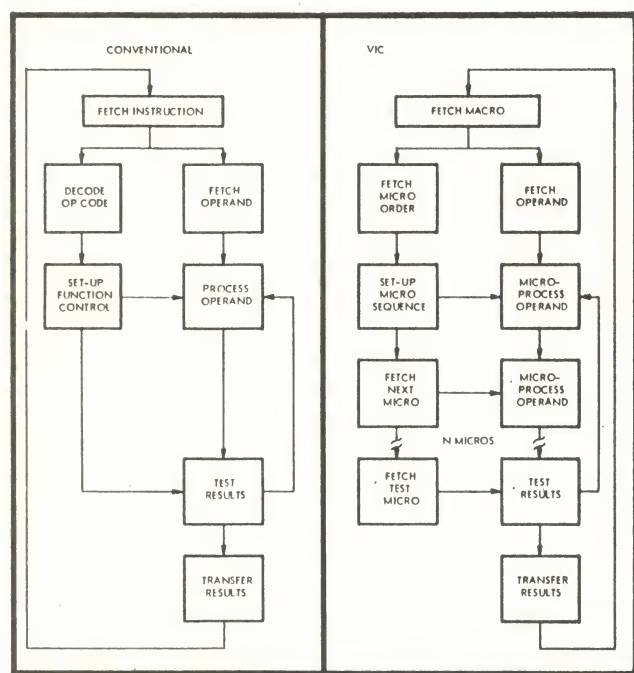


Figure 1. Concept Comparison

RCA - USAF VIC-36A

The work to build a research model of the VIC began in the spring of 1965. The objective was to demonstrate the VIC concept by utilizing off-the-shelf components wherever possible. To complement the unique reliability aspects of the VIC approach, integrated circuits, organizational

modularity, and checking features were built into the model.

Figure 2 summarizes the VIC-36A specifications. A key feature is the flexibility which provides the user with several different number systems. For reliability, the variable instructions are stored in the redundant high speed memory modules. To provide for future growth, the main memory is expandable in 4K modules up to 32 thousand words. The four independent input/output channels are built into a traffic control system having four levels of priority.

- GENERAL PURPOSE, 36 BIT PARALLEL, STORED PROGRAM
- 1 AND 2's COMPLEMENT, FIXED POINT SIGN AND MAGNITUDE, HEXADECIMAL FLOATING POINT
- 67,000 AVERAGE OPERATIONS PER SECOND
- UP TO 128 DUPLEX VARIABLE INSTRUCTION LOCATIONS
- TWO 256 x 38 BIT WORD 0.6 MICROSECOND HIGH SPEED MEMORIES
- TWO (TO EIGHT) 4096 x 38 BIT WORD 3.0 MICROSECOND MAIN MEMORY MODULES
- FOUR INPUT AND OUTPUT CHANNELS (1-36 BIT, 3-8 BIT)
- 200 Kc PARALLEL INPUT/OUTPUT RATE

Figure 2. VIC-36A Specifications

The physical configuration of the VIC central processor unit is shown in Figure 3. Each sub-assembly may be removed for repair including the power supply modules and the high speed core memory stacks. Cooling is achieved by metal thermal conductive paths from the silicon semiconductor to a cold plate mounting surface. The size, weight, and power figures include the duplex 400 cycle ac power supplies. Figure 4 shows the main memory unit with only two of the four 4096 word main memory modules installed. The size, weight, and power figures include the full 16K word complement. Connectors are provided for connecting a second 16K word main memory unit. With the full complement of 32K words of storage, the expanded 36-bit parallel word VIC-36A is 4.4 cubic feet and weighs 175 lbs. These size and weight figures include all of the reliability features and redundant circuits described in this paper.

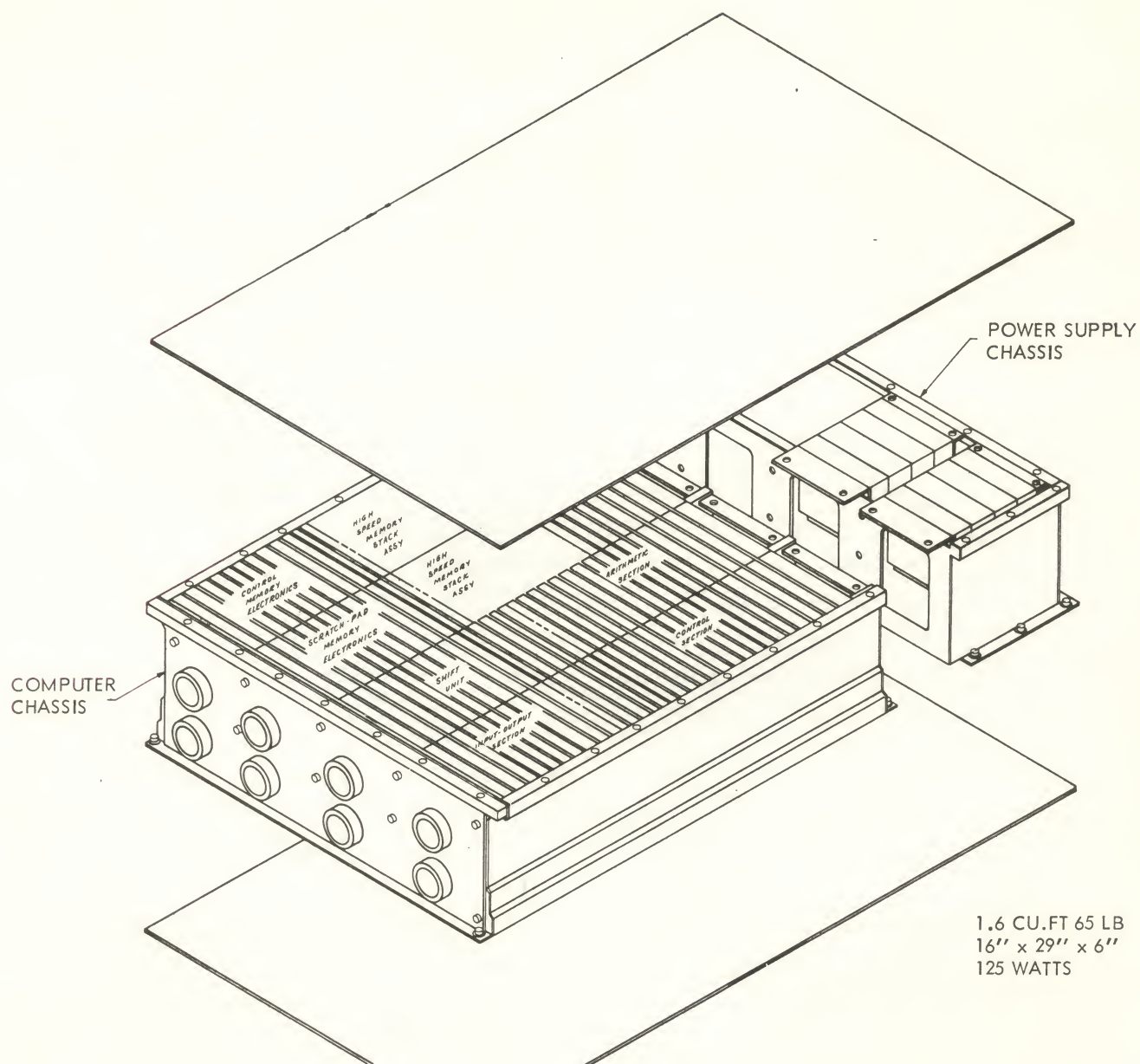


Figure 3. Central Processor Unit

Objectives

The objectives of this paper are (1) to describe the VIC-36A at the block diagram level, (2) discuss its intrinsic reliability features and (3) show how the VIC concept extends the basic reliability by means of algorithm change in order to achieve multiple levels of graceful degradation.

Technical Discussion

Components and Construction

The VIC design utilizes integrated circuits in order to benefit from the high reliability afforded by fewer components and interconnections. In Figure 5, three of the main memory data register cards are shown in the column on the left. Note the 8 monolithic silicon integrated sense amplifiers and the 8 DTL flip-flop register flat packs. The two cards in the

last row in the upper right hold 8 dual hybrid switch circuit packages and the associated decoding logic flat packs. The remaining card in the last row holds the four main current driver cordwood modules required for one of the 4096 x 38 bit main memory modules. The large heat-conducting flange assures that the heat generated by the drivers is conducted to the heat sink. The driver card and the load resistor card in the rear column, next to last row, are the only assemblies besides the power supply modules which do not contain integrated circuits.

Each card is guided by tracks in the metal column separators. The metal strips at the top edge of each card make intimate contact with the cold plate which covers the unit. Each card is secured to the column separators by a screw at each end of the metal strip. The total thermal drop from the active component junction to the cold plate surface is less than 25° centigrade.

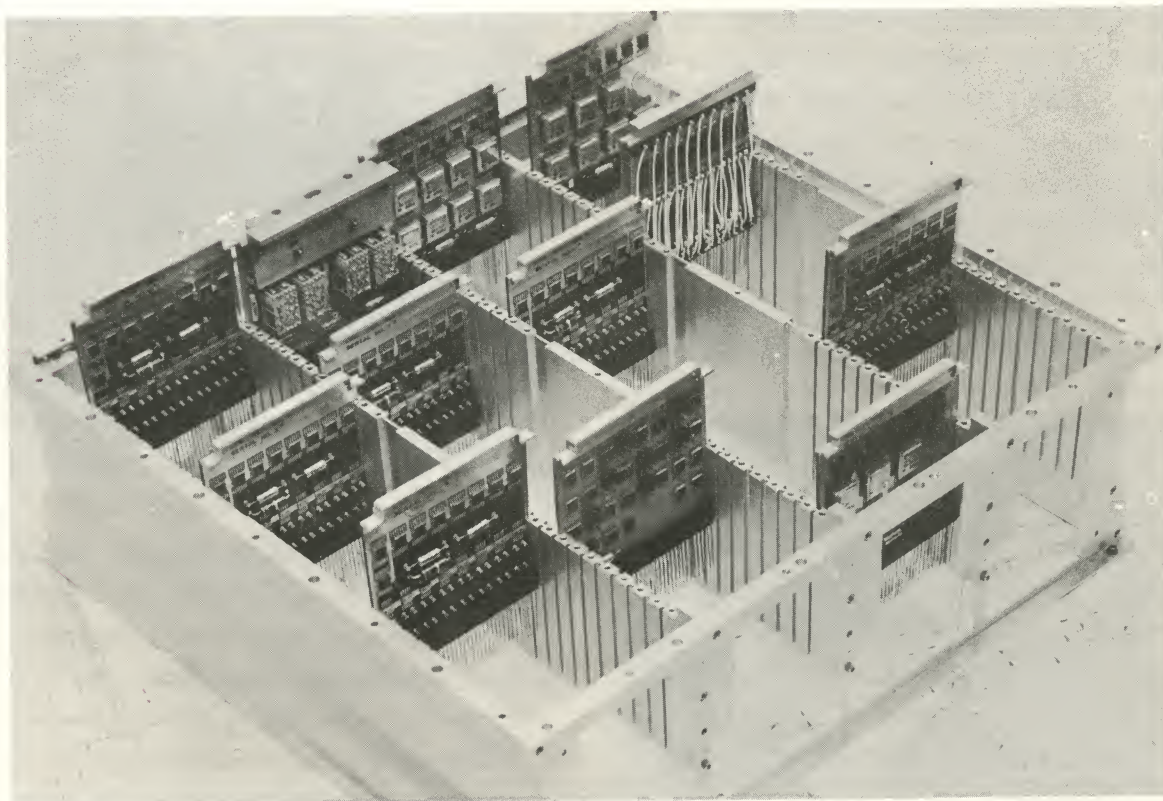


Figure 5. Main Memory Assembly

Tests performed on this type of construction have proven its ability to withstand environmental hazards encountered in both air and spacecraft. For maintainability, each card is directly accessible and its planar construction allows component test and repair with simple test equipment and shop tools.

In choosing the memory approach for VIC the goal was reliable operation over a 125°C temperature range with minimum susceptibility to stray magnetic fields and power supply transients. To meet these requirements, the device selected was the closed magnetic path Toroidal core, made of wide temperature lithium ferrite, developed by RCA at Needham, Mass. Its characteristics are essentially flat over any 100°C temperature range below the curie point. Operation is extended to 125°C by modifying the interrogate current as a function of core stack temperature.

Figure 6 is a photograph of the VIC high speed memory stack which operates on a 600 nanosecond cycle. The four modes in which the memory operates are: clear/write, read/restore, read/modify/write, or read/count/write cycle. The high speed memory is organized as a two-core-per-bit linear select memory. It provides 325 nanosecond parallel access to any of the 256 x 38 bit words. A 30 millivolt bipolar readout from the two 20 x 12 mil cores provides an extremely reliable readout signal.

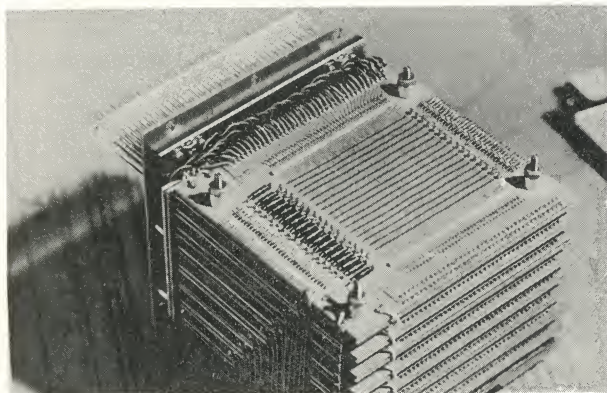


Figure 6. High-Speed Memory Stack

The main memories employ 30 x 18 mil lithium ferrite cores operating in a coincident current mode. They provide a 3.0 microsecond clear/write, read/restore, or read/modify/write cycle time and an access time of 650 nanoseconds. A typical readout signal is 60 millivolts and the sense amplifier threshold level is greater than 10 mV at -55°C and greater than 30 mV at +100°C.

Both memories utilize silicon monolithic integrated circuit sense amplifiers. The current switches are hybrid integrated circuit units which utilize thin film interconnection techniques. Each switch is transformer-coupled and two circuits are packaged in a single 0.75 inch square hermetically sealed package.

Figure 7 illustrates a typical logic circuit card. Each card is 3.75 x 3.5 inches and can accommodate up to 32 integrated circuit packages. The cards are either 4-layer built-up plated circuit cards or 3-layer welded wire matrix assemblies.

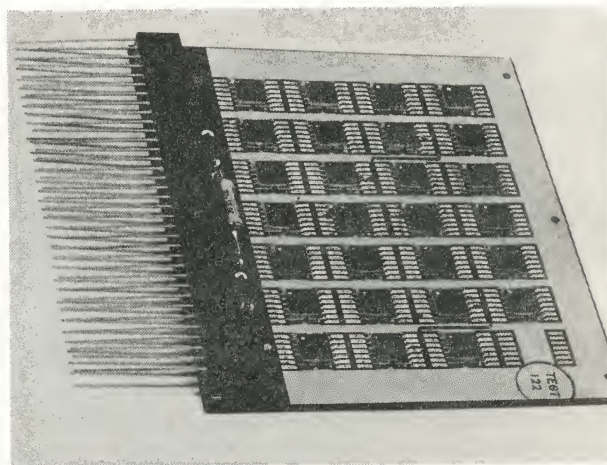


Figure 7. Logic Card

Both types utilize the same 70-pin connector. The long beryllium copper pins on the connector are designed to pass through a multi-layer welded matrix backplane as shown in Figure 8A. After the card is inserted in the backplane, the long connector pin is adjacent to a similar pin which is welded to the wires within the backplane as shown in Figure 8B. The

adjacent pins are then wire-wrapped together to produce an extremely reliable connection which can withstand extremes of shock, vibration, and temperature. At the point of maximum compression, as shown in Figure 8C, the metals recrystallize and fuse into a very low impedance connection at four points in every turn of the wrap. As a result, the resistance of a wire-wrap connection is only 0.0007 ohm, compared to 0.006 ohm for a typical solder joint and 0.01 ohm for a typical connector pin. The wire wraps may

between those used for military equipments and those required on the Minuteman high reliability program. Interconnection techniques improve as they progress from solder to welding to wire wrap. In each case, rigid NASA procedures and tests verify the workmanship. Connectors are the least reliable, as their failure rate indicated, and the effect of their virtual elimination in the VIC and the effects on reliability are significant.

With the data derived in Figure 9, it is now possible to determine the improvements attained

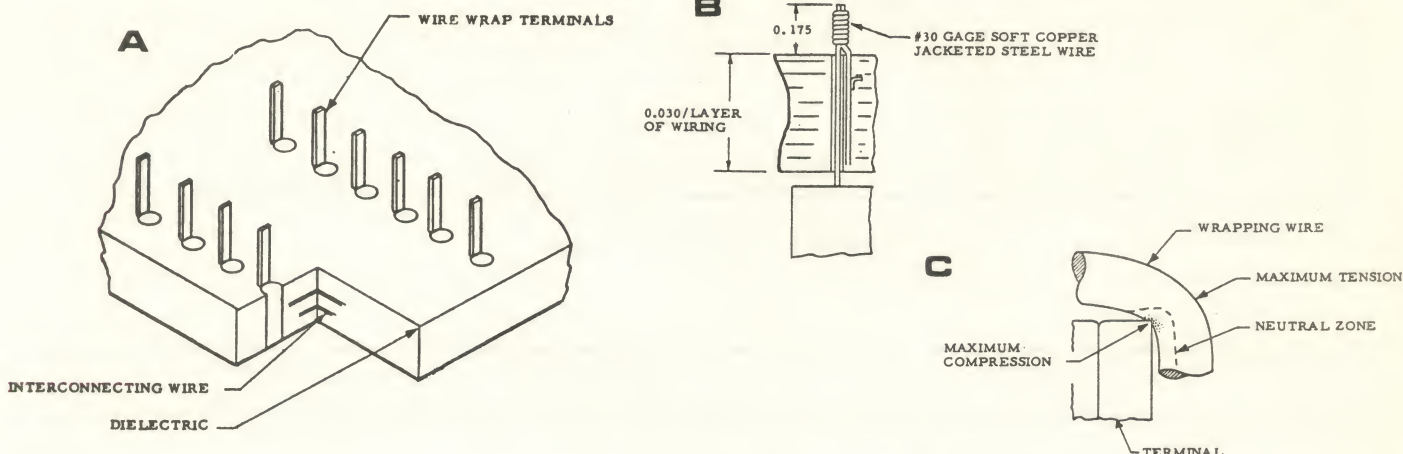


Figure 8. Split Pin Wiring Wrap - Wiring Module

be removed and discarded and new wraps may be installed as often as required.

The VIC interconnection technique also provides the reliability of a solid-encapsulated welded-wire backplane. The backplane is built layer-by-layer from welded wire matrices which are individually inspected and tested. These are assembled and welded to pins in a step-by-step process with inspections and tests at each step. The entire assembly is then encapsulated in a solid unit.

Basic Reliability Predictions

After that introduction to the VIC, its components and construction, the next step is to determine the basic reliability factors based on component counts and straightforward redundancy. Figure 9 shows the VIC-36A failure rate analysis for each section of the computer. The part failure rates are typical of those utilized on the Lunar Excursion Module (LEM) program. The rates fall

by the use of simple redundancy in VIC. Figure 10 shows the effects of redundancy on the MTBF of VIC, assuming that no repair is possible during a simple mission.

The first four columns of Figure 10 show the MTBF for a single thread VIC of 4K, 8K, 16K, and 32K words of main memory to be 2400, 2000, 1500, and 1000 hours, respectively. In the next four columns, as a result of having duplex high memory, control registers, and central processor power supply an improvement of from 30% to 10% in MTBF is gained, depending on the amount of main memory capacity. In the last four columns, as a result of having a spare main memory and its associated power supply, an improvement of from 75% to 70% is gained over the single thread case, depending on the amount of main memory capacity required. The hardware cost in terms

	FAILURE RATE λ^*	ARITHMETIC UNIT		CONTROL UNIT		INPUT-OUTPUT		HIGH SPEED MEMORY		POWER SUPPLY		4K MAIN MEMORY		MAIN MEMORY PS	
		n	n λ	n	n λ	n	n λ	n	n λ	n	n λ	n	n λ	n	n λ
DIGITAL I.C.'S	0.10	774	77.4	950	95.0	500	50.0	266	26.6			222	22.2		
ANALOG I.C.'S	0.30							45	13.5			40	12.0		
HYBRID CIRCUITS	0.40							104	41.6			53	21.2		
TRANSISTORS	0.06							4	0.2	32	1.9	4	0.2	22	1.3
DIODES	0.03							116	3.5	84	2.5	512	15.4	41	1.2
CAPACITORS	0.02			19	0.4	9	0.2	93	1.9	66	1.3	63	1.2	21	0.4
RESISTORS	0.002							166	0.3	120	0.2	111	0.2	58	0.1
TRANSFORMERS	0.20									9	1.8			8	1.6
SOLDER JOINTS	5.0×10^{-4}	7700	3.8	9500	4.8	5000	2.5	4900	2.5	750	0.4	4600	2.4	350	0.2
WELDS	2.0×10^{-4}	2300	0.5	2800	0.5	1400	0.3	800	0.2			70	0.1		
WIRE WRAPS	4.0×10^{-5}	2100	0.1	2400	0.1	1260	0.1	1680	0.1	780	—	1540	0.1	280	—
STACK	1.6							1	1.6			1	1.6		
CONNECTORS	(0.001/PIN)					70	0.07			20	—	70	0.07	20	—
TOTALS			81.8		100.9		53.3		92.0		8.1		76.7		4.8

* λ = FAILURES/ 10^6 HRS.

Figure 9. MTBF Analysis

	m λ	SINGLE THREAD				DUPLEX HSM, VR, CR & PS				DUPLEX HSM & PS			
	F/ 10^6 HRS	4K	8K	16K	32K	4K	8K	16K	32K	4K/8K	8K/12K	16K/20K	32K/36K
CENTRAL PROCESSOR													
ARITHMETIC	81.8	81.8				81.8				81.8			
CONTROL	90.9	90.9				90.9				90.9			
CR AND VR	10	10				*							
INPUT-OUTPUT	53.2	53.2				53.2				53.2			
HIGH SPEED MEMORY	92.0	92.1				*							
POWER SUPPLY	8.1	8.1				*							
TOTAL CPU		336	336	336	336	236	236	236	236	236	236	236	236
MAIN MEMORY													
4K + PS	81.9	82				82				*			
8K + PS	163.8		164				164				98		
16K + PS	327.6			328				328				180	
32K + PS	655.2				655				655				347
TOTAL m λ		418	500	664	991	308	390	554	881	236	334	416	583
MTTF = m λ / 10^6		2400	2000	1500	1000	3200	2550	1800	1100	4200	3000	2400	1700

* INSIGNIFICANT BY VIRTUE OF REDUNDANCY.

Figure 10. Effects of Redundancy on MTBF

of size or weight for the 75% improvement in MTBF was only 20% while for the 70% improvement in the 32K word machine it was only 12.5%.

These basic reliability predictions show the effects of employing integrated circuits, core

memory devices, and advanced packaging techniques to yield good basic reliability in VIC. The use of switchable redundant modules was discussed to show how VIC's basic MTBF can be effectively improved simply by a nominal increase in hardware. A discussion of what unique additional

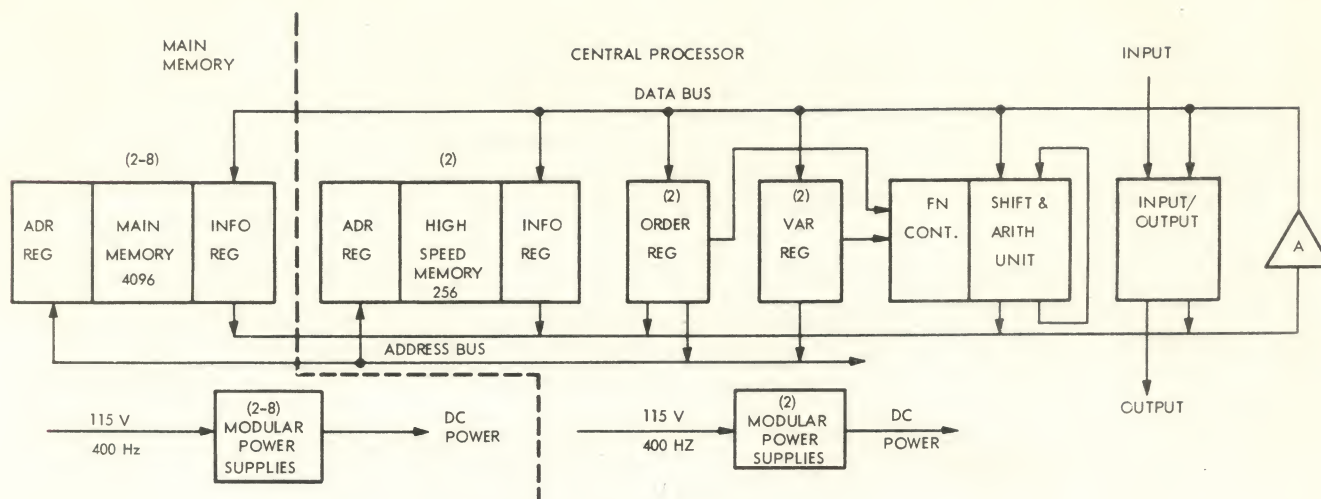


Figure 11. Organization

reliability features accrue from the use of the variable instruction technique follows.

VIC Block Diagram

The RCA/USAF VIC has an unusual modular organization as shown in Figure 11. Each major functional unit is as nearly independent of other units as possible. For example, each of the main memory modules has its own independent address register, information register, local control and power supply. Each of the two high speed memory modules has the same independent features. There are two independent power supplies in the central processor either of which can serve the entire processor. The two pairs of order and variable registers, whose function will be described later, are also independent of each other. There are four input/output channels each separately addressable and independent of each other. The function control, shift, and arithmetic units will be treated later.

As indicated in Figure 11, the VIC is organized around two busses, one for data and the other for address information. Each of these busses is uni-directional and, thus, a single set of amplifiers can service all data transfers. Test data on a large number of monolithic integrated diode-transistor-logic circuits of the type used in the VIC shows that 95% of the failures in these circuits occur in a condition where all circuit impedance is removed from the input or output terminals. Thus a condition in which the VIC bus "hangs up" and cannot be switched by the surviving circuitry is highly improbable.

Figure 12 shows all the circuits in one main memory module. All of the essential circuits are included; in addition, a parity generator in the central processor generates a parity bit for every word as it is sent to memory. When either the main or high speed memory is accessed, a parity check is performed in the central processor. Thus a failure of any component in a memory module will be detected when the affected location is accessed.

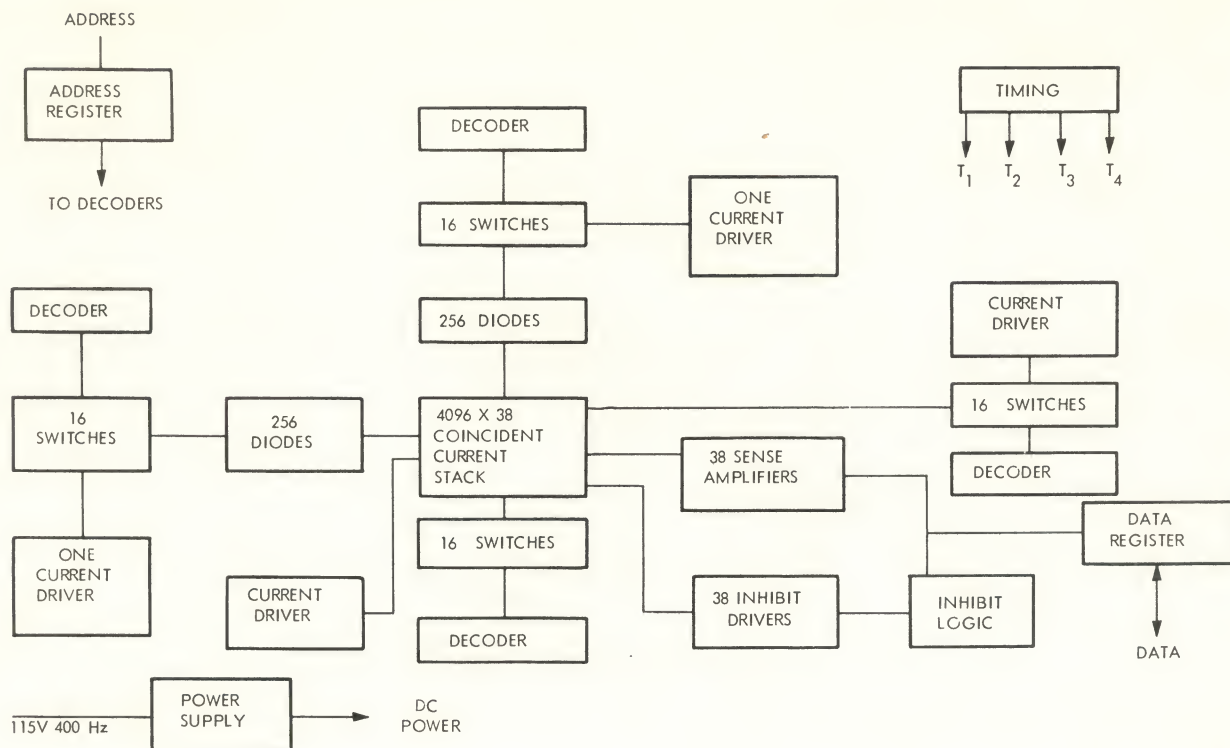


Figure 12. Main Memory

The arithmetic unit is shown in Figure 13. The data bus interface is indicated at the top and bottom of the diagram. Two control lines are shown coming in from the left. The arithmetic unit is organized in a vertical slice so that two bits of each of the three double-rank registers and two bits of the arithmetic and logic section are all on a single card. This card is the one shown in Figure 7. There are eighteen of these cards in the full 36-bit arithmetic unit.

The variable instructions control the arithmetic unit. All the shift, arithmetic, logical, and interim storage functions are controlled by discrete bits in the variable instruction word. Figure 14 lists all of the functions which can be performed in the arithmetic and logic unit. Each of these functions is independent and separate from the others and may be called out by the micro orders in a wide variety of ways. Making each of these operations as simple and basic as possible gives the programmer complete freedom to design an almost unlimited set of macro orders.

Figure 15 shows all of the circuits in one of the high speed memory modules. The failure of a component in either module will be detected by the check on parity as every affected word is read out of the module just as with the main memory modules. One high speed memory module is a duplicate of the other as shown in Figure 16. Note that one half the memory is devoted to variable word storage, one quarter to program counters and input/output control, and one quarter to scratch pad storage. In normal operation only

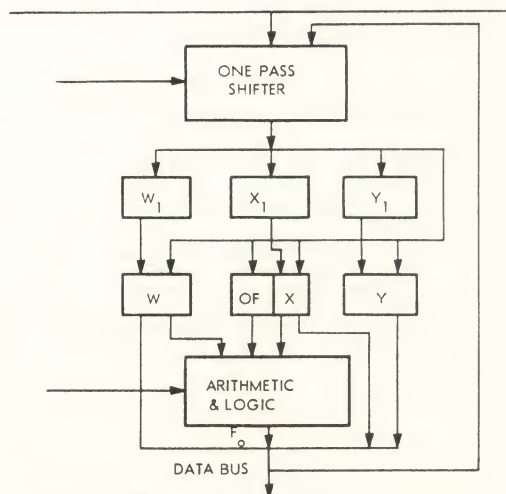


Figure 13. Arithmetic Unit

CODE	FUNCTION	REMARKS	CODE	FUNCTION	REMARKS
000000	$W \text{ OR } X$		010000	$C(X) - 1$	DECREMENT X BY 1
000001	$\overline{W} \text{ AND } \overline{X}$		010001	$(C(X) - 1) [\overline{Y}_{35}]$	DECREMENT X BY 1 IF Y_{35} IS 0
000010	$\overline{W} \text{ OR } X$		010010	$ C(X) + 1$	COMPLEMENT MAGNITUDE OF C(X) AND INCREMENT BY 1
000011	$W \text{ AND } \overline{X}$		010011	$ C(X) $	COMPLEMENT MAGNITUDE OF C(X)
000100	$W \text{ OR } \overline{X}$		010100	$C(X) + 1$	INCREMENT X BY 1
000101	$\overline{W} \text{ AND } X$		010101	$(C(X) + 1) [Y_{35}]$	INCREMENT X BY 1 IF Y_{35} IS 1
000110	$\overline{W} \text{ OR } \overline{X}$		010110	DIVIDE STEP	
000111	$W \text{ AND } X$		010111	MULTIPLY STEP	
001000	$W \oplus X$	EXCLUSIVE OR	011000	SPECIAL ADD	TWO'S COMPLEMENT ADD: $X \Sigma_2 W$ WITH FORCED CARRY
001001	$\overline{W} \oplus \overline{X}$		011001	$X \Sigma_2 W$	ADDITION: TWO'S COMPLEMENT
001010	$\overline{X}$		011010	$X \Sigma_1 W$	ADDITION: ONE'S COMPLEMENT
001011	X		011011	$X -_1 W$	SUBTRACTION: ONE'S COMPLEMENT
001100	$\overline{W}$		011100	$X -_2 W$	SUBTRACTION: TWO'S COMPLEMENT
001101	W		011101	SPECIAL SUBTRACT	SUBTRACT: $X -_2 W$, NO CARRY IN
001110	0	ALL ZEROES	011110	$X \Sigma_{sm} W$	ADDITION: SIGN, MAGNITUDE
001111	1	ALL ONES	011111	$X -_{sm} W$	SUBTRACTION: SIGN, MAGNITUDE

Figure 14. Arithmetic & Logic Unit Functions

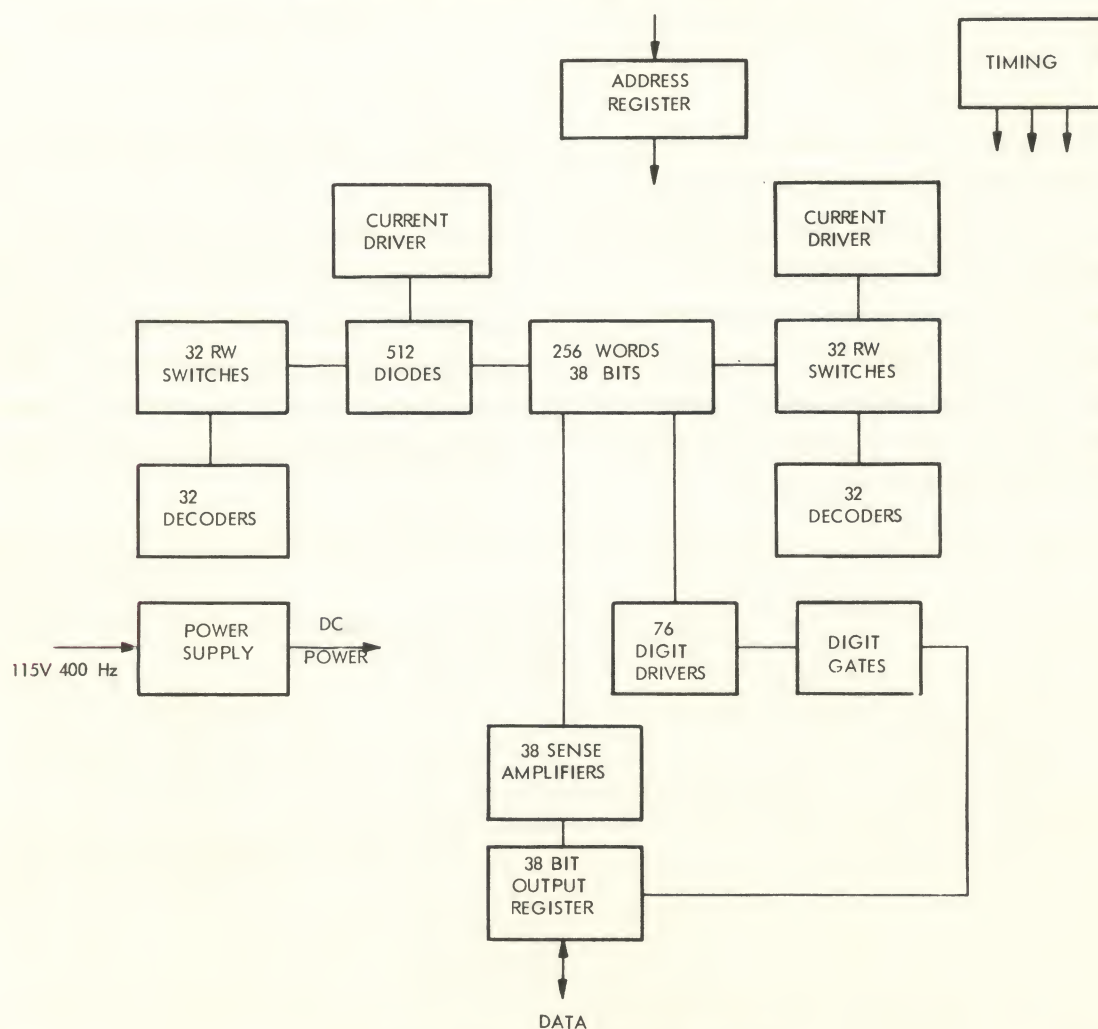


Figure 15. High Speed Memory

one of the high speed memory modules is interrogated at one time. If an error is detected, the second module is interrogated. If the second module is read incorrectly, a diagnostic routine is called in and information may be restored from non-volatile back-up store, if necessary. Whenever the information in a scratch pad or program counter location is changed, both modules are updated simultaneously.

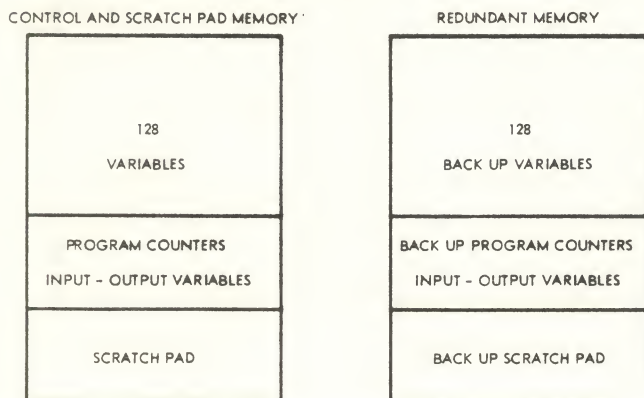


Figure 16. High Speed Memory Allocation

Figure 17 shows the VIC control unit. The redundant order registers receive the macro order from the main memory. The redundant variable registers receive the micro orders from the control memory. The bit content of these two registers is decoded in: (1) the data control to set up the data transfer paths in the machine; and (2) in the test, function and address control to set up the number of shifts, the

functions to be executed, the number of iterations and the type of tests to be performed. The signals thus generated go to the transfer gates, shift unit, arithmetic and logic unit, program counters, and input/output variable storage locations.

VIC is unique in that it is an asynchronous machine and there is no central clock source which is critical to the operation of the separate functional units. Such clock sources are usually non-redundant and involve a few components which are heavily loaded by drive current power requirements. Central clock sources are also heavily dependent upon the reliability of inter-connection techniques and freedom from local EMI sources and power supply transients.

Power Supply Features

There are two types of ac to dc power supplies in the VIC. One is for a 4096 word main memory module, and one is for a high speed memory module and the central processor unit. Both types have the same block diagram shown in Figure 18. The 400 Hz input power is rectified, filtered, and then chopped at a 10 kHz rate. The 10 kHz square wave drives a small power transformer with multiple secondary windings. These develop

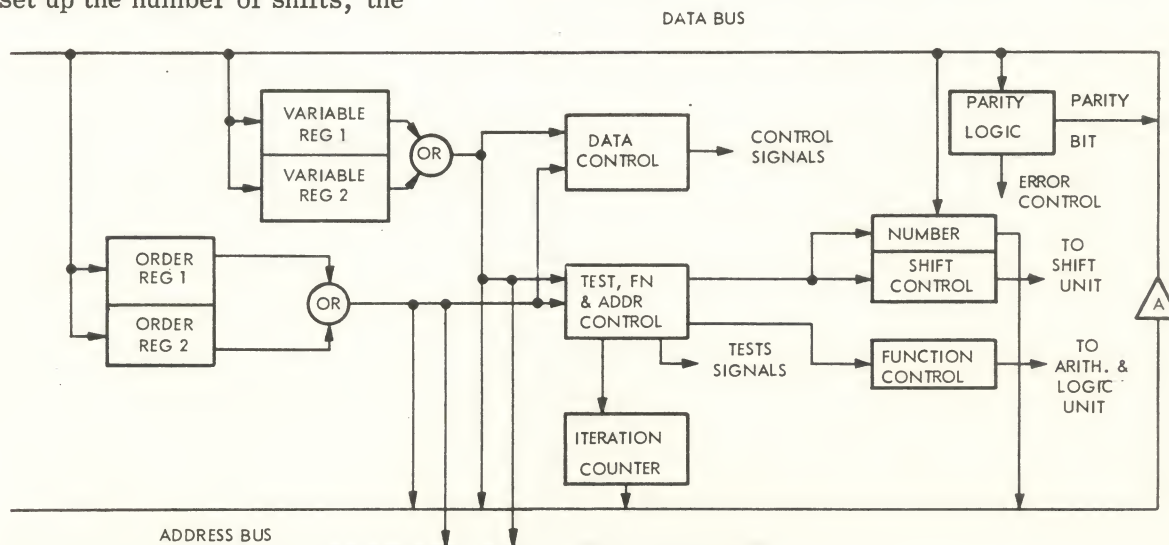


Figure 17. Control Unit

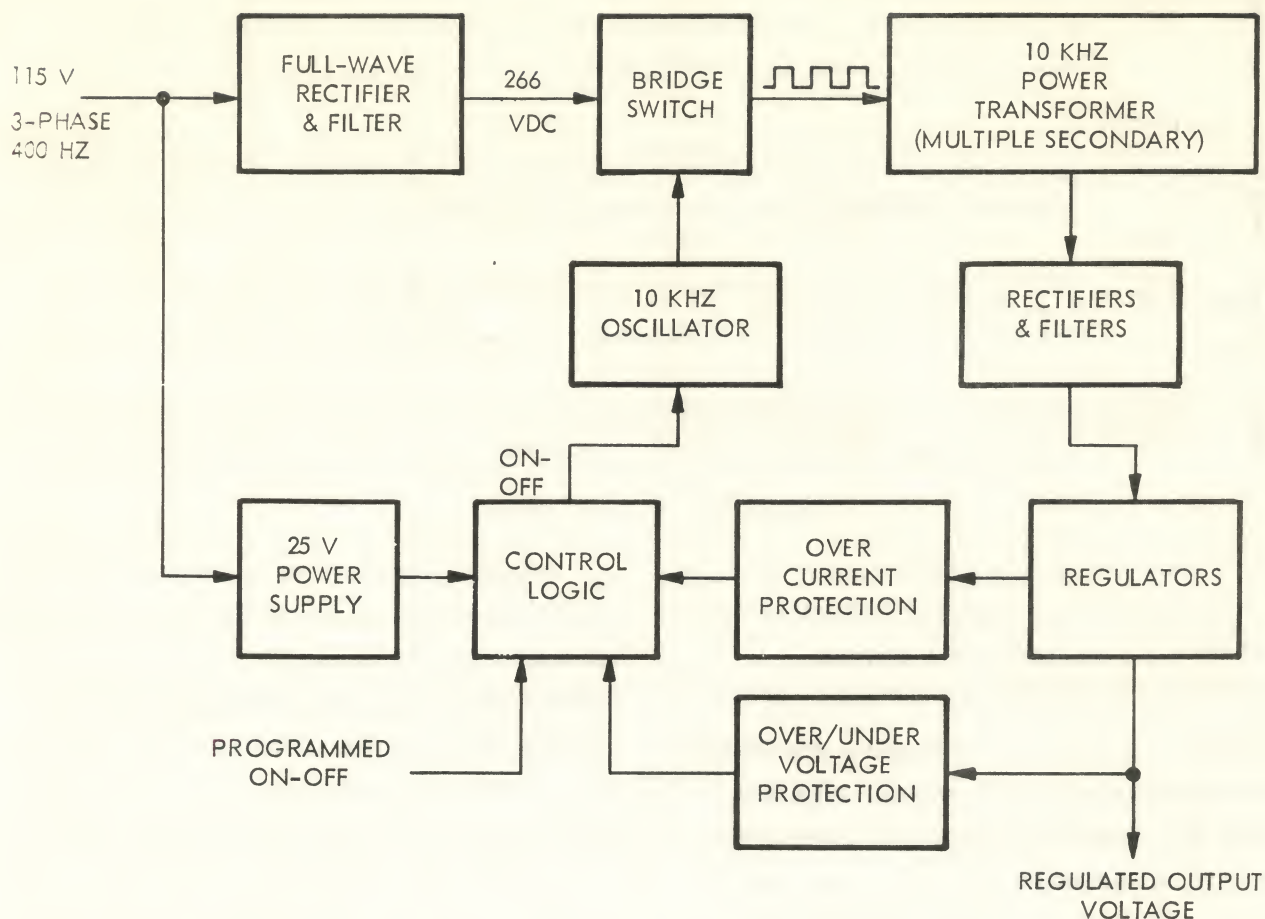


Figure 18. VIC Power Supplies

the various input amplitudes for a set of rectifiers, filters, and regulators for each of the dc output voltages required. The regulator outputs are sensed for overcurrent, overvoltage, and undervoltage. These go-no-go signals are used to initiate a fast stop action in the 10 kHz oscillator control logic. This control logic also enables the programmer to turn off excess memory capacity during certain phases of the mission. This increases the longevity of the memory modules and enables them to survive excessive temperature and radiation extremes.

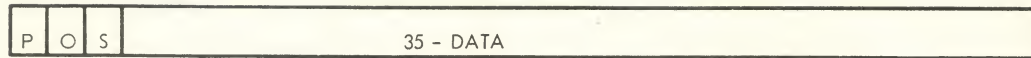
Variable Instruction Technique

Now that we have described the circuits, construction, organization and standard reliability aspects of the VIC, we can discuss the unique reliability features of the VIC. Figure 19

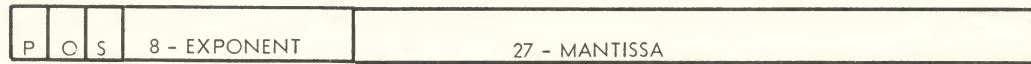
shows the word formats used in the VIC. The program or macro instruction operation code is, in part, the address of the first variable word in control memory. The variable word contains three 12-bit micro orders which control the discrete micro operation of the VIC.

The way in which the program and variable words are combined to control the step-by-step operation of the VIC is illustrated in Figure 20. The bits of the order register and variable register are decoded to generate specific data address and control operations. At least one and sometimes four or five variable words are required for each order. Since every variable contains three micro orders, a macro order may have 12 or 15 micro orders. Because of the great flexibility of the VIC transfer paths, arithmetic, logical and shift operations, a macro can be

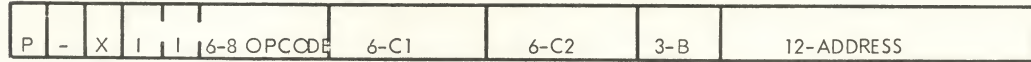
FIXED
POINT
DATA



FLOATING
POINT DATA



PROGRAM



VARIABLE



Figure 19. Word Formats

formulated from micros in a wide variety of ways. Herein lies the fundamental advantage of the VIC from the standpoint of reliability.

Given this most flexible set of computer parameters, a programmer can find a great many ways to execute a particular macro. With this flexibility it is possible to substitute alternative ways to execute an order and circumvent the failure of some portion of every register and control path in the machine. A comprehensive set of diagnostics can be formulated which can detect failures in basic algorithms and then determine which secondary or even tertiary algorithms can be substituted.

Suppose, for example, that the second bit of the adder logic has suffered a permanent fault. Then the data can be treated as two half words, and the addition can be performed in two steps in the good half of the arithmetic unit. Alternatively, the words to be added can be converted to their complement, subtracted and the result re-completed. Even though these alternatives will require more time, the computer can continue to operate. The micro routine for the add operation would be permanently altered so that every time a macro calls for an add operation the altered micro sequence will be used.

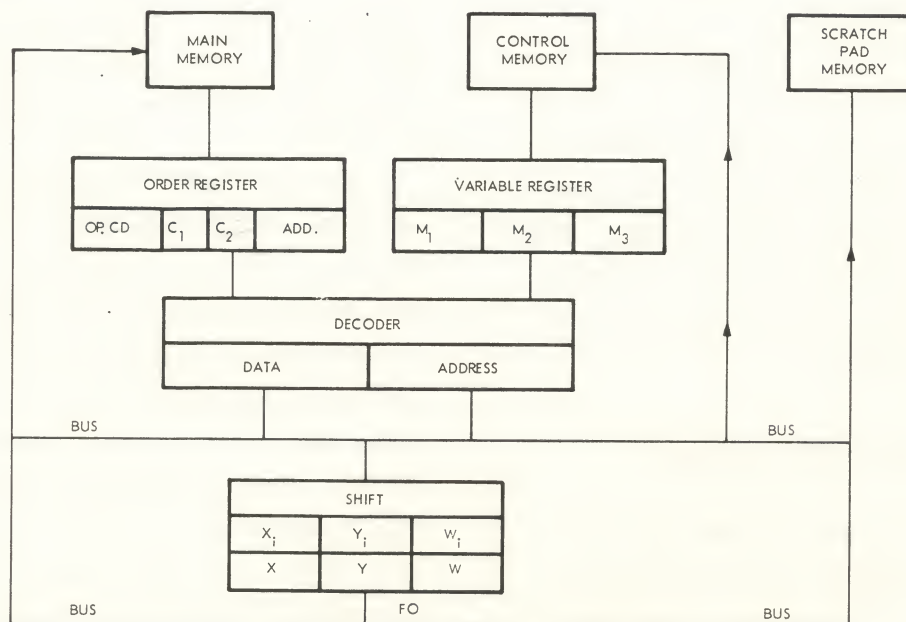


Figure 20. Instruction Flow

It is reasonable to consider a 36-bit parallel arithmetic unit as three 12-bit units which normally operate in parallel. If one, or even two, of these 12-bit bytes have failed, it is still possible to continue operating on a 12-bit byte. This is sometimes called "graceful degradation" or the multithreading* approach to reliability. The given analysis in the referenced paper shows that this approach has particular merit where high meantime before failure goals are required and repair is not possible.

Summary

A model of a variable instruction computer has been built which demonstrates the ability of the variable technique to enhance reliability by means of controlled graceful degradation. The features built into the VIC include independent memory modules, redundant control memories

and registers, asynchronous operation and independent I/O channels. In addition, the variable instruction technique provides a means for on-line algorithm substitution to achieve multiple modes of operation each at successively lower levels of degradation. (See Figure 21).

Conclusions

The variable instruction computer is a unique approach to achieving a reliable aerospace computer. It provides a higher reliability for critical tasks by a multithread technique to achieve graceful degradation.

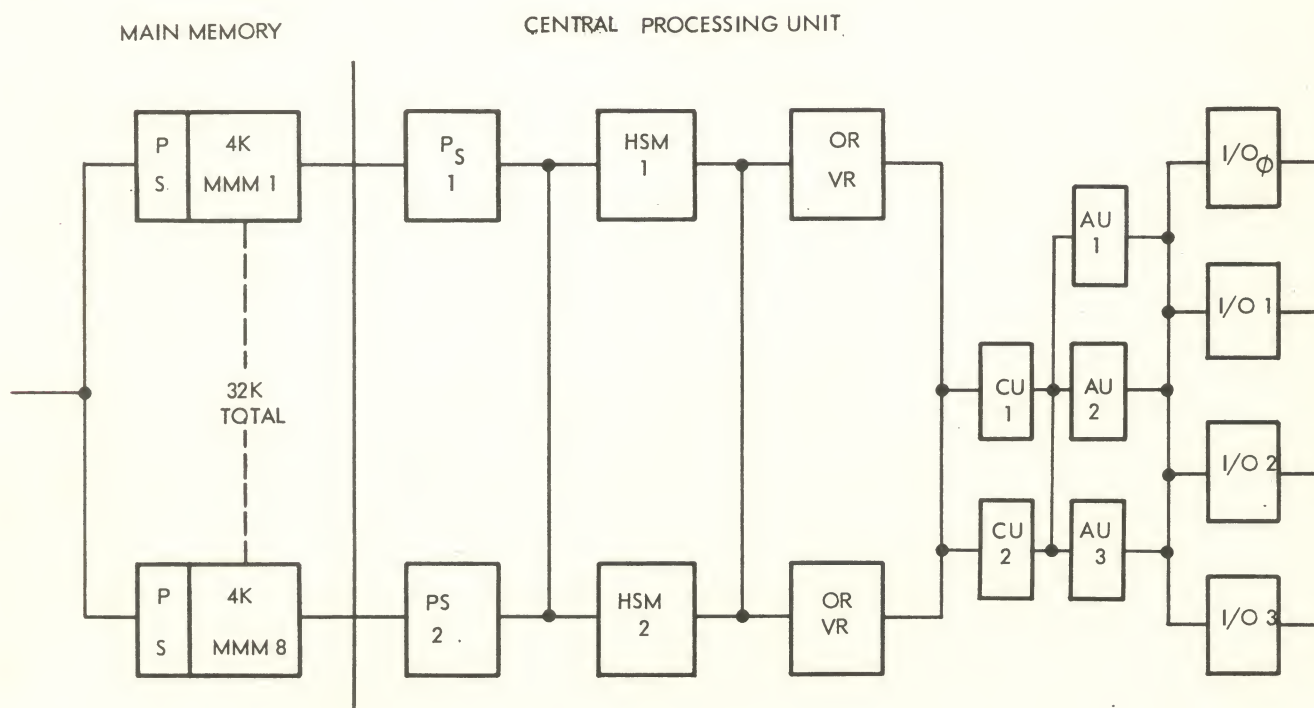


Figure 21. Reliability Block Diagram

*See, for example, "Multithreading Design of a Reliable Aerospace Computer", R. P. Hassett and E. H. Miller, Radio Corporation of America, Burlington, Mass; 1966 Aerospace and Electronic Systems Convention Proceedings, May 3-5, 1966